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Research on the Mechanism of Neutral-point Voltage Fluctuation and Capacitor Voltage Balancing Control Strategy of Three-phase Three-level T-type Inverter

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Abstract – In order to solve the neutral-point voltage fluctuation problem of three-phase three-level T-type inverters (TPTLTIs), the unbalance characteristics of capacitor voltages under different switching states and the mechanism of neutral-point voltage fluctuation are revealed. Based on the mathematical model of a TPTLTI, a feed-forward voltage balancing control strategy of DC-link capacitor voltages error is proposed. The strategy generates a DC bias voltage using a capacitor voltage loop with a proportional integral (PI) controller. The proposed strategy can suppress the neutral-point voltage fluctuation effectively and improve the quality of output currents. The correctness of the theoretical analysis is verified through simulations. An experimental prototype of a TPTLTI based on Digital Signal Processor (DSP) is built. The feasibility and effectiveness of the proposed strategy is verified through experiment. The results from simulations and experiment match very well.

Keywords: Fluctuation characteristics, Mechanism of neutral-point voltage fluctuation, T-type three-level inverter, Voltage difference feed-forward balancing control

1. Introduction

In a three-phase three-level T-type inverter (TPTLTI), the midpoint of the DC capacitors is connected to the phase inductors through bidirectional switches (e.g. insulated-gate bipolar transistors, IGBTs) which guarantee the three-level output voltages [1, 2]. Comparing with conventional two-level inverters, TPTLTIs have the following advantages: 1) low switching losses and high efficiency; 2) the small *dv/dt* produced by the switches leads to less electro-magnetic noises; 3) the three-level output voltages contain less harmonics which reduces the size of phase inductors and the corresponding power losses and costs. Therefore, TPTLTIs are widely used in photovoltaic power generation, wind power generation, motor drive and other low-voltage and cost-sensitive applications [3-5].

However, TPTLTIs also have some shortcomings, for instance, it needs more switches and its control algorithms are complex. The voltage unbalance of DC capacitors is also a typical problem in TPTLTIs [6]. Ideally, the voltage of each capacitor is half of the DC bus voltage. However, the charge or discharge of the two DC capacitors are not synchronous under practical operating conditions, which makes the voltages of the two capacitors unequal, causes the fluctuations of the capacitor neutral-point and ultimately deteriorates the output currents. In addition, the imperfections of the DC capacitors and the inconsistent characteristics of switching devices can further worsen the voltage unbalance of the capacitors [7]. One of the DC capacitors and the switches in the corresponding arms will withstand a high DC voltage once the capacitor voltages become severely unbalanced. Thus, the lifetime of capacitors and switches will be reduced, which can eventually damage the capacitors and switches.

The unbalance of capacitor voltages is a common problem in neutral-point clamped (NPC) three-level inverters. Many researches have been carried out on this problem. Researchers have proposed many capacitor balancing control methods. Reference [8] uses the reference DC voltage and load currents to represent the mean value of the neutral current and derives a neutral-point voltage control model. The analysis in [8] shows that the unbalance of capacitor voltages is due to the current flowing through the DC capacitors. The neutral-point voltage control can be achieved through controlling the average neutral current to be zero and keeping DC voltage invariant in each control period. Essentially, the neutral-point voltage control strategy controls the switching vectors (redundant switching states) and thereby controls the zero sequence components of the average output voltages to be zero. A new neutral-point voltage control algorithm, so called “prediction - calibration - correction”,

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is proposed in [8]. However, the algorithm is not suitable to be applied in TPTLTIs due to its heavy computational complexity. In order to control the neutral-point voltage of TPTLTIs, another control strategy which replaces N-type or P-type small switching states with other switching states is proposed in [9]. The strategy has a strong capability of controlling the neutral-point voltage in the conditions of pure reactive power mode and over modulation mode. However, it increases the THD of output currents and needs to judge the directions of phase currents accurately, which increases the difficulty and complexity of control. Although references [8] and [9] proposed neutral-point voltage balancing control algorithms, the principles of the variations of capacitor voltages under different switching states are not revealed. The mechanism of the unbalance of capacitor voltages in a single-phase three-level inverter is analyzed and a neutral-point voltage control strategy is proposed in [10]. However, the mathematical expressions of capacitor neutral-point voltage are different between single-phase three-level inverters and TPTLTIs. Hence, the analysis and control strategy for single-phase three-level inverters cannot be applied to TPTLTIs directly.

In [11], a neutral-point voltage control algorithm for low-voltage ride-through operation of a three-level inverter is proposed. However, this paper only considers influence of middle vectors on the neutral-point voltages and its control. The impacts of small vectors are not taken into account. A hybrid pulse width modulation-based discontinuous modulation strategy with DC-link voltage balancing for a NPC three-level traction inverter drive is proposed in [12]. Considerable reductions of the harmonic distortions of the inverter voltages and currents are achieved through the proposed strategy which also reduces the capacitor voltage unbalances to considerable levels. Nonetheless, the strategy is only suitable for off-grid inverters, not for grid-connected inverters.

In this paper, the neutral-point voltage fluctuation characteristics and the mechanism of capacitor voltage unbalance in different switching states are revealed. According to the switching states of TPTLTIs, six typical circuits are analyzed. The state equations of the circuits are derived and the expressions of the DC-link capacitor voltages are obtained. A feed-forward voltage balancing control strategy of DC-link capacitor voltages error is proposed. The strategy generates a DC bias voltage using a capacitor voltage loop with a proportional-integral (PI) controller. This paper is organized as follows. Section II derives the mathematical model of a TPTLTI. Section III analyses the fluctuation characteristics of capacitor voltages under different switching states. The mechanism of the neutral-point voltage fluctuation of a TPTLTI is investigated as well. Section IV proposes a feed-forward voltage balancing control strategy of DC-link capacitor voltages error for TPTLTIs based on the neutral-point voltage fluctuation mechanism. The simulation and experimental results verifying the effectiveness and advantages of the proposed method are presented in Section V. Section VI gives conclusions and closes the paper.

2. Mathematical Model and Modulation Principle of TPTLTIs

2.1 Mathematical model of TPTLTIs

The topology of a TPTLTI is shown in Fig. 1. TPTLTIs are extended from conventional two-level inverters. It contains three clamped branches composed by front-to-front connecting switches T_{x3} and T_{x4} (x=A, B, C) between the neutral-point of each phase and the DC capacitor neutral-point. There are three voltage levels ($-V_{dc}/2$, 0 and $V_{dc}/2$) at the AC side of TPTLTIs. "P", "0" and "N" are used to represent three working states of the three output voltage levels, respectively [1, 13].

Each phase of a TPTLTI contains four switches (T_{x1}-T_{x4}). T_{x1} and T_{x2} cannot be in conducting states at the same time to avoid short-circuits. It is the same to T_{x1} and T_{x4} (T_{x2} and T_{x3}). Considering the above constraints, the switches (T_{x1}, T_{x4}) and (T_{x2}, T_{x3}) are treated as two switch pairs (two switches in a pair are simultaneously turned on and off). One of the two switch pairs is always on. The switching function is defined as follows.

$$S_x = \begin{cases} 1, & T_{x1} = T_{x3} = \text{ON} \\ 0, & T_{x3} = T_{x4} = \text{ON} \\ -1, & T_{x2} = T_{x4} = \text{ON} \end{cases} \quad (1)$$

where, x=A, B, C.

The output phase voltages are:

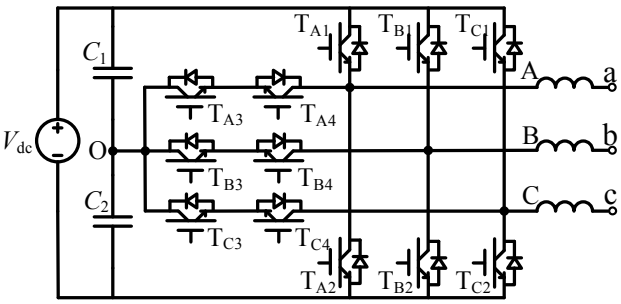


Fig. 1. The topology a TPTLTI

Table 1. Output voltage levels and switching states of a TPTLTI

Working conditions	Switching States				S_x	Output voltage levels
	T_{x1}	T_{x2}	T_{x3}	T_{x4}		
P	on	off	on	off	1	V_{dc} /2
0	off	off	on	on	0	0
N	off	on	off	on	-1	$-V_{dc}$ /2

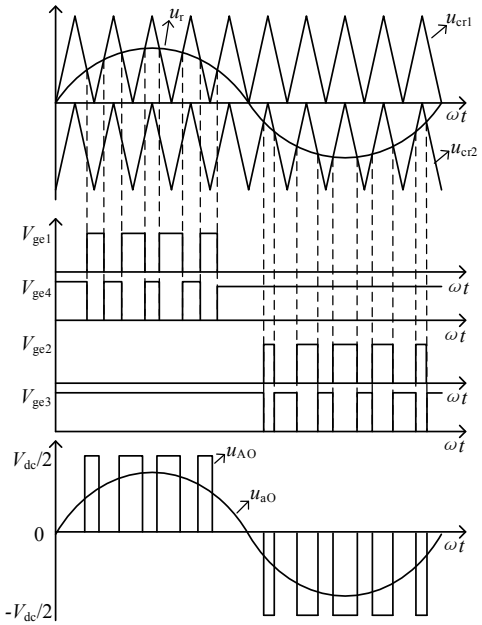


Fig. 2. The principle of the dual-carrier phase disposition SPWM strategy

$$u_{x0} = S_x \frac{V_{dc}}{2} \tag{2}$$

Accordingly, the relationship between the output voltage levels and the switching states of a TPTLTI is obtained in Table 1 [6].

The output voltages of a TPTLTI can be expressed through S_x and V_{dc}:

$$\begin{bmatrix} u_{AO} \\ u_{BO} \\ u_{CO} \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} S_A \\ S_B \\ S_C \end{bmatrix} \tag{3}$$

2.2 Modulation principles of TPTLTIs

Four firing signals are needed to trigger the four switches in each phase of TPTLTIs. Dual-carrier phase disposition sinusoidal-pulse-width-modulation (SPWM) strategy can generate four firing signals by comparing a modulation wave with two carriers. The principle of the dual-carrier phase disposition SPWM strategy is shown in Fig. 2, where u_{cr1} and u_{cr2} are carrier waves, and u_r is modulation wave. Two complementary pulse-width-modulation (PWM) signals V_{ge1} and V_{ge4} are generated by comparing u_r with u_{cr1} to drive T_{A1} and T_{A4}. Similarly, V_{ge2} and V_{ge3} are generated by comparing u_r with u_{cr2} to drive T_{A2} and T_{A3}. The outputs of V_{ge1} and V_{ge2} can be presented as follows [14, 15]

$$V_{ge1} = \begin{cases} 1, u_r > u_{cr1} \\ \text{Hold}, u_r = u_{cr1} \\ 0, u_r < u_{cr1} \end{cases} \tag{4}$$

$$V_{ge2} = \begin{cases} 0, u_r > u_{cr2} \\ \text{Hold}, u_r = u_{cr2} \\ 1, u_r < u_{cr2} \end{cases} \tag{5}$$

3. E Analysis of Neutral-point Voltage Fluctuations of TPTLTIs

In a TPTLTI, each phase has three switching states: "P", "0" and "N". There are 27 switching states of the three phases. The space vectors of the 27 switching states in $\alpha\beta$ frame are shown in Fig. 3 [16, 17]. According to the magnitudes of the vectors, the space vectors can be divided into four categories as shown in Table 2.

The circuit of a TPTLTI will be a NPC inverter during medium and small vectors wherein the unequal currents flow through the two capacitors and results in the unbalance of capacitor voltages. The severity of the unbalance depends on the current amplitudes and the duration of the NPC circuits. A typical NPC circuit with a medium vector of "P0N" is depicted in Fig. 4(a). Similarly, typical NPC circuits with positive small vectors of "P00" and "PP0" are depicted in Fig. 4(b) and (c). Fig. 4 (d) and (e) illustrate typical NPC circuits with negative small vectors of "0NN" and "00N". Fig. 4 (f) shows a typical circuit with large vector of "PNN".

In Fig. 4, assuming R_1=R_2=R_3=R, L_1=L_2=L_3=L, and C_1=C_2=C, the following equations can be derived according to Fig. 4 (a).

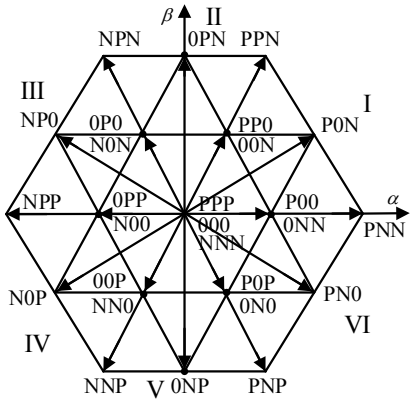
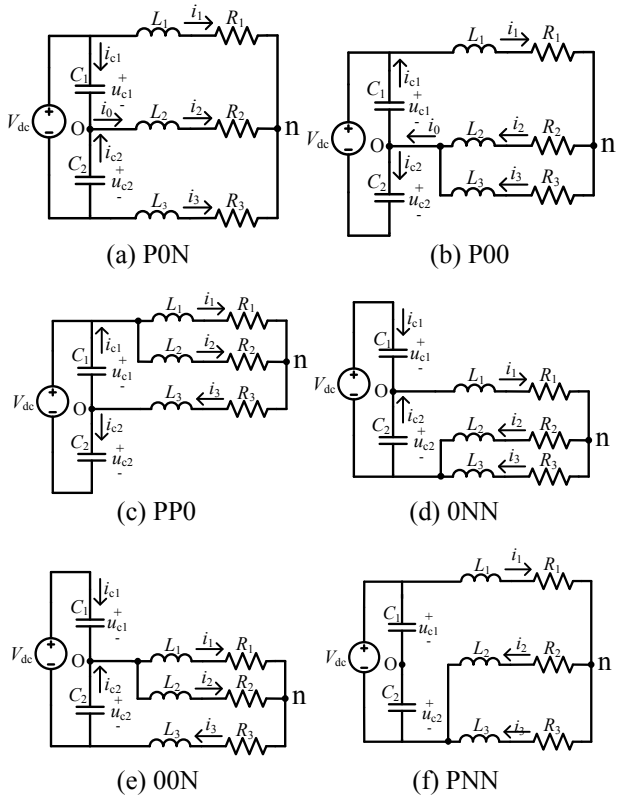


Fig. 3. Space vectors of a TPTLTI

Table 2. Categories of the space vectors of a TPTLTI.

Categories		Space Vectors	Magnitudes
Large Vectors		$\vec{U}_{PNN}, \vec{U}_{PPN}, \vec{U}_{NPN}, \vec{U}_{NPP}, \vec{U}_{NNP}, \vec{U}_{PNP}$	V_{dc}
Medium Vectors		$\vec{U}_{P0N}, \vec{U}_{0PN}, \vec{U}_{NP0}, \vec{U}_{N0P}, \vec{U}_{0NP}, \vec{U}_{PN0}$	$\sqrt{3}\ V_{dc}/2$
Small Vectors	Positive	$\vec{U}_{P00}, \vec{U}_{PP0}, \vec{U}_{0P0}, \vec{U}_{0PP}, \vec{U}_{00P}, \vec{U}_{P0P}$	Small Vectors
	Negative	$\vec{U}_{0NN}, \vec{U}_{00N}, \vec{U}_{N0N}, \vec{U}_{N00}, \vec{U}_{NN0}, \vec{U}_{0N0}$	
Zero vectors		$\vec{U}_{PPP}, \vec{U}_{000}, \vec{U}_{NNN}$	0



(a) P0N (b) P00 (c) PP0 (d) 0NN (e) 00N (f) PNN

Fig. 4. Typical NPC circuits structures with medium, small and large vectors

$$\begin{cases} i_1 + i_2 + i_3 = 0 \\ u_{c1} + u_{c2} = V_{dc} \\ C\dfrac{du_{c1}}{dt} - C\dfrac{du_{c2}}{dt} = i_0 = i_2 \\ L\dfrac{di_1}{dt} + Ri_1 - Ri_2 - L\dfrac{di_2}{dt} = u_{c1} \\ L\dfrac{di_1}{dt} + Ri_1 - Ri_3 - L\dfrac{di_3}{dt} = V_{dc} \end{cases} \tag{6}$$

From (6), the state equations of i_0 and u_{c1} can be obtained as:

$$\begin{bmatrix} \dfrac{di_0}{dt} \\ \dfrac{du_{c1}}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{R}{L} & -\dfrac{2}{3L} \\ \dfrac{1}{2C} & 0 \end{bmatrix} \begin{bmatrix} i_0 \\ u_{c1} \end{bmatrix} \tag{7}$$

From (7), i_0 and u_{c1} can be derived as

$$\begin{cases} i_0(t) = A_1 e^{\alpha_1 t} + A_2 e^{\alpha_2 t} \\ u_{c1}(t) = U_{c1(0)} + \dfrac{1}{2C}\int i_0(t)dt \end{cases} \tag{8}$$

where, A_1 and A_2 are the coefficients determined by the initial values of capacitor voltages and inductor currents, and $\alpha_{1,2}$ is:

$$\alpha_{1,2} = \frac{-\dfrac{R}{L} \pm \sqrt{\dfrac{R^2}{L^2} - \dfrac{4}{3LC}}}{2} \tag{9}$$

Similarly, the following equations can be derived according to Fig. 4 (b).

$$\begin{cases} i_1 = i_0 = i_2 + i_3 \\ u_{c1} + u_{c2} = V_{dc} \\ i_0 = -C\dfrac{du_{c1}}{dt} + C\dfrac{du_{c2}}{dt} \\ L\dfrac{di_1}{dt} + Ri_1 + Ri_2 + L\dfrac{di_2}{dt} = u_{c1} \\ L\dfrac{di_1}{dt} + Ri_1 + Ri_3 + L\dfrac{di_3}{dt} = u_{c1} \end{cases} \tag{10}$$

From (10), the state equations of i_0 and u_{c1} can be obtained as:

$$\begin{bmatrix} \dfrac{di_0}{dt} \\ \dfrac{du_{c1}}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{R}{L} & \dfrac{2}{3L} \\ -\dfrac{1}{2C} & 0 \end{bmatrix} \begin{bmatrix} i_0 \\ u_{c1} \end{bmatrix} \tag{11}$$

From (11), i_0 and u_{c1} can be derived as:

$$\begin{cases} i_0(t) = B_1 e^{\beta_1 t} + B_2 e^{\beta_2 t} \\ u_{c1}(t) = U'_{c1(0)} - \dfrac{1}{2C}\int i_0(t)dt \end{cases} \tag{12}$$

where, B_1 and B_2 are the coefficients determined by the initial values of capacitor voltages and inductor currents, and $\beta_{1,2}$ is:

$$\beta_{1,2} = \frac{-\dfrac{R}{L} \pm \sqrt{\dfrac{R^2}{L^2} - \dfrac{4}{3LC}}}{2} \tag{13}$$

From (8) and (12), it can be seen that the value of the neutral-point current is determined by the circuit parameters, initial capacitor voltages and inductor currents. The variations of capacitor voltages are determined by the directions of the neutral-point current. The variations of capacitor voltages are determined by the value and duration of the neutral-point current and the capacitance.

According to (8), the relationship between the variations of the directions of capacitor voltages and the neutral-point current in Fig. 4 (a) can be obtained as follows:

Condition 1: When i_0 flows out of the neutral-point, u_{c1} increases;

Condition 2: When i_0 flows into the neutral-point, u_{c1} decreases.

According to (12), the capacitor voltage u_{c1} will decrease,

Table 3. Capacitor voltage variations of TPTLTI

Variation Rule	i_0	Operating States
u_{c1} increases, u_{c2} decreases	flowing out of the neutral-point	0NN, 00N, N0N, N00, NN0, 0N0 P0N, 0PN, NP0, N0P, 0NP, PN0
u_{c1} decreases, u_{c2} increases	flowing into the neutral-point	P00, PP0, 0P0, 0PP, 00P, P0P P0N, 0PN, NP0, N0P, 0NP, PN0
u_{c1}, u_{c2} keeps invariant	=0	PNN, PPN, NPN, NPP, NNP, PNP, PPP, 000, NNN

when the TPTLTI is operating at the state of "P00" and i_0 is flowing into the neutral-point, as shown in Fig. 4(b).

Similarly, the variations of u_{c1} and u_{c2} in other states can be obtained. The variations rule of u_{c1} and u_{c2} in all states of the TPTLTI are shown in Table 3.

4. Feed-forward Voltage Balancing Control Strategy of DC-link Capacitor Voltages Error

The modulation waves, carrier waves and firing signals in one carrier period are shown in Fig. 5(a) when the dual-carrier phase disposition SPWM strategy is employed. The firing signals (T_{A1}, T_{A2}, T_{B1}, T_{B2}, T_{C1}, T_{C2}) are produced by comparing the three-phase modulation waves (u_{ra}, u_{rb}, u_{rc}) and the two carrier waves (u_{cr1} and u_{cr2}). Assuming i_a>0, i_b<0 and i_c>0, according to Table 3, the variations of the capacitor voltages u_{c1} and u_{c2} of the 7 states of the TPTLTI are also illustrated in Fig. 5(a).

t_1−t_7 are the durations of the 7 states of the TPTLTI in one carrier period. Assuming the average value of the neutral-point current is I_0 except during t_2 and t_6. Thus, the variations of u_{c1} in one carrier period can be expressed as:

$$\Delta u_{c1} = \frac{1}{C}(-t_1 - t_3 + t_4 - t_5 - t_7) \cdot abs(I_0) \tag{14}$$

In order to balance the capacitor voltages, u_{c1} should be decreased and u_{c2} should be increased if $u_{c1} > u_{c2}$ at t_k. Therefore, a DC bias voltage u_o can be added to the modulation waves to change the duration of each state, which will change the charging or discharging durations of the capacitor voltages and therefore control the neutral-point voltage to be stable. Assuming the DC bias voltage u_o > 0, the modulation waves after adding the DC bias voltage can be expressed as:

$$u'_{rx} = u_{rx} + u_o \tag{15}$$

where, x=A, B, C.

After adding u_o, the modulation waves, carrier waves and firing signals in one carrier period are shown in Fig. 5(b). In order to simplify the analysis, it is assumed that the change of the PWM signals before and after adding the DC bias voltage is Δt. Therefore, the durations of each state become as follows:

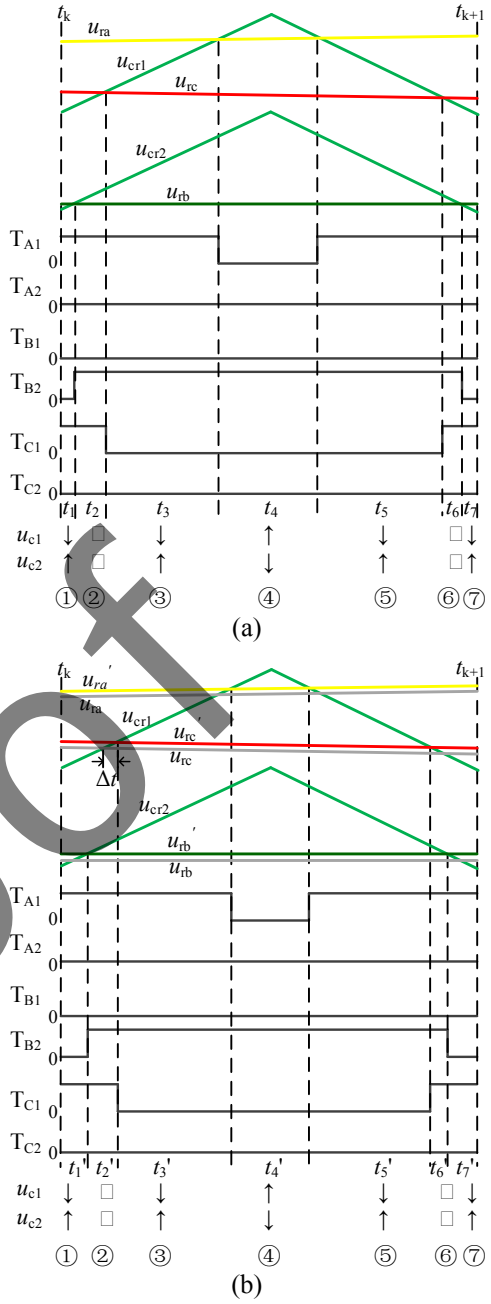


Fig. 5. The PWM signals in one carrier period. (a) original modulation wave, (b) modulation wave with DC bias voltage ("↑" : u_c increases; "↓" : u_c decreases; "-": u_c keeps invariant)

$$\begin{cases} t_1' = t_1 + \Delta t \\ t_2' = t_2 - \Delta t + \Delta t = t_2 \\ t_3' = t_3 - \Delta t + \Delta t = t_3 \\ t_4' = t_4 - \Delta t - \Delta t = t_4 - 2\Delta t \\ t_5' = t_5 + \Delta t - \Delta t = t_5 \\ t_6' = t_6 + \Delta t - \Delta t = t_6 \\ t_7' = t_7 + \Delta t \end{cases} \tag{16}$$

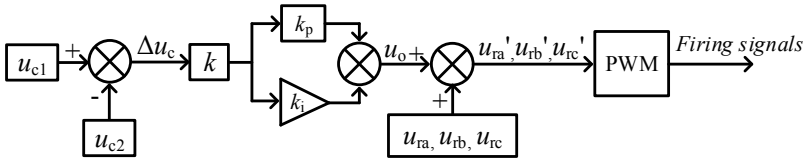


Fig.6. The schematic diagram of the voltage difference feed-forward balancing control strategy

After adding DC bias voltage, the variation of u_{c1} in one carrier period can be expressed as:

$$\Delta u_{c1}^{'} = \frac{1}{C}(-t_1 - t_3 + t_4 - t_5 - t_7 - 4\Delta t) \cdot abs(I_0) \qquad (17)$$

The difference between $\Delta u'_{c1}$ and Δu_{c1} can be obtained as

$$\Delta u_{c1}^{'} - \Delta u_{c1} = \frac{1}{C}(-4\Delta t) \cdot abs(I_0) \qquad (18)$$

According to (18), in one carrier period after adding the DC bias voltage, the increases of u_{c1} is $\frac{1}{C}(4\Delta t) \cdot abs(I_0)$, which accelerates the balance of the capacitor voltages.

Similarly, u_{c1} will decrease $\frac{1}{C}(4\Delta t) \cdot abs(I_0)$ after adding the negative DC bias voltage when $u_{c1} < u_{c2}$.

According to the above analysis, a feed-forward voltage balancing control strategy of DC-link capacitor voltages error is proposed. Fig. 6 shows the schematic diagram of the control strategy, where u_{ra}, u_{rb} and u_{rc} are the original modulation waves, Δu_c is the difference value between u_{c1} and u_{c2} which will be processed through a PI controller to get the DC bias voltage u_o. The value of the new modulation waves u_{ra}', u_{rb}' and u_{rc}' can be obtained by adding u_o to the original modulation waves. The new modulation waves contain a DC component which could balance the capacitor voltages. The new modulation waves are sent to PWM to produce the firing signals.

The proposed voltage balance control strategy can be easily implemented only by detecting the capacitor voltages. No need to measure the neutral-point current and determine the operating states of switches. No need of additional devices which saves the costs.

5. Simulation and Experimental Results

5.1 Simulation results

In order to verify the correctness of the analysis of the neutral-point voltage fluctuations and the effectiveness of the capacitor voltage difference feed-forward balancing control strategy, a TPTLTI model is built in PSCAD/ EMTDC, as shown in Fig. 7. The dual-carrier phase disposition SPWM strategy is employed. The parameters of the model are given in Table 4. Simulations were carried out under dynamic changes of output currents and different power factors (PFs).

Table 4. The parameters of the TPTLTI Model

Parameters	Symbol	Value
DC voltage	V_{dc}	800V
AC voltages	e_a, e_b, e_c	220V
Rated capacity	S_N	10kVA
Smoothing inductors	L_1, L_2, L_3	10mH
Carrier frequency	f_s	2kHz
Fundamental frequency	F	50Hz
Gain coefficient	k	0.2
Proportional coefficient	k_p	3
Integral coefficient	k_i	0.1

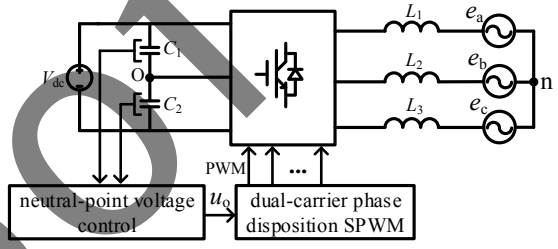
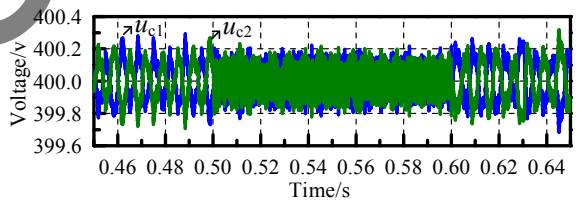
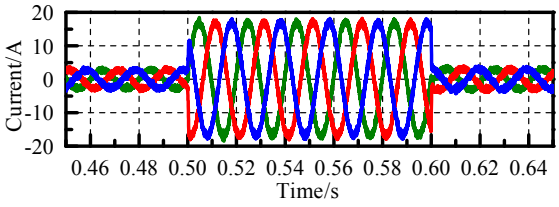


Fig.7. The schematic diagram of the TPTLTI model



(a)



(b)

Fig. 8. Simulation results with different output currents: (a) DC capacitor voltages; (b) Inverter output currents

5.1.1 Simulations under dynamic changes of output currents

The proposed capacitor voltage balancing control is

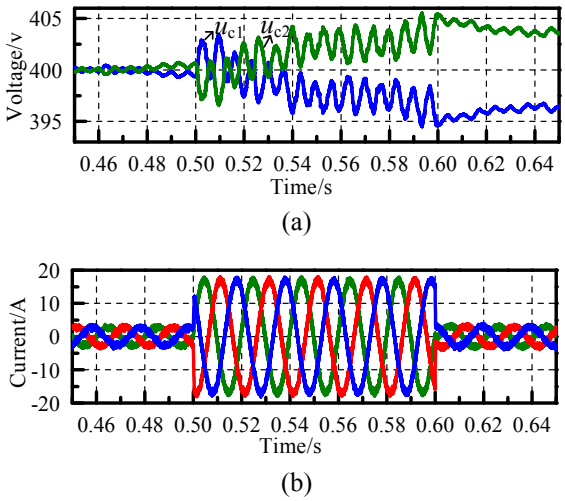


Fig. 9. The dynamic responses without the proposed strategy: (a) DC capacitor voltages; (b) Inverter output currents

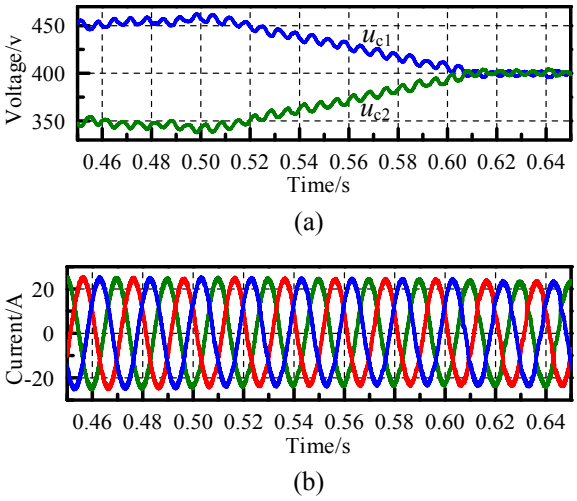


Fig.10. The dynamic responses under PF=0.1: (a) DC capacitor voltages; (b) Inverter output currents

applied in this case study. Inverter output current changes to 12 A from 2 A at 0.5 s and changes back to 12 A at 0.6 s. As shown in Fig. 8(a), the performance of the proposed strategy is not affected by the dynamic changes of the inverter output currents. The fluctuations of u_{c1} and u_{c2} are kept within 0.4 V. It can been seen from Fig. 8(b), the output currents are not distorted when the TPTLTI operates within the rated capacity with the proposed strategy.

Fig. 9 shows the case without applying the proposed strategy. Compared to the last case, the unbalance of u_{c1} and u_{c2} becomes worse and cannot recover. The maximum voltage difference between u_{c1} and u_{c2} increased to around 10 V.

5.1.2. Simulations under different PFs

Fig. 10 shows the dynamic responses of the proposed strategy with a PF of 0.1. The capacitor voltage balancing control is triggered at 0.5 s. As shown in Fig. 10(a), the capacitor voltages become balanced within 100 ms. The average voltage difference between u_{c1} and u_{c2} reduces to 0 V. The inverter output currents are shown in Fig. 10(b), which are not distorted with the proposed strategy.

Fig. 11 illustrates the dynamic responses of the proposed strategy under a unit PF. capacitor voltage balancing control is triggered at 0.5 s. As shown in Fig. 11(a), the capacitor voltages become balanced within 0.003 ms. The average voltage difference between u_{c1} and u_{c2} reduces to 0 V. The inverter output currents are shown in Fig. 10(b), which are not distorted with the proposed strategy.

Fig. 11(c) and 11(d) are the (Fast Fourier Transform) FFT results of the inverter currents without and with the neutral-point voltage control in the case of PF=1. The THDs are 3.25% and 3.09%, respectively.

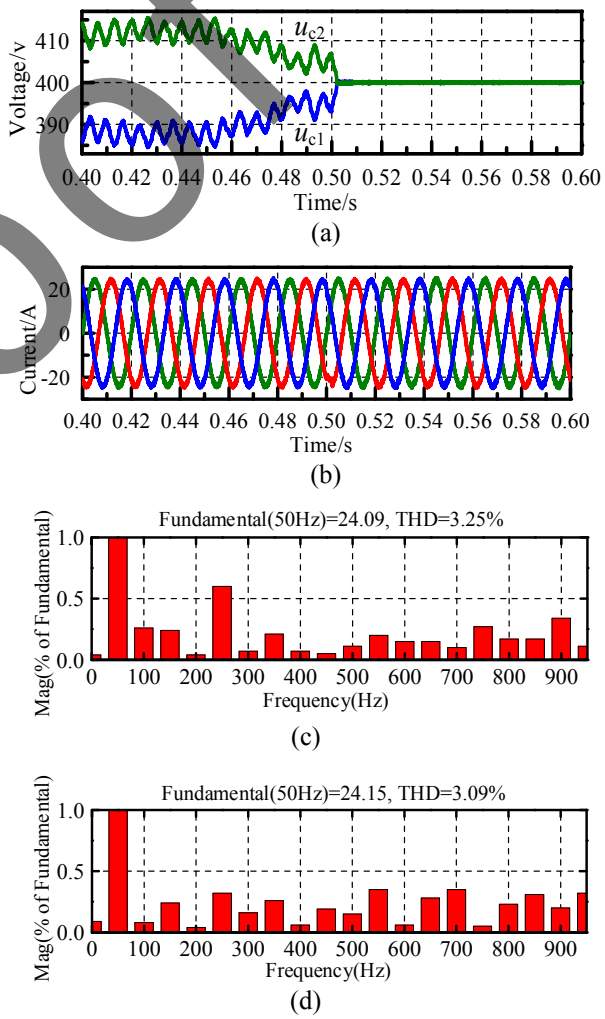
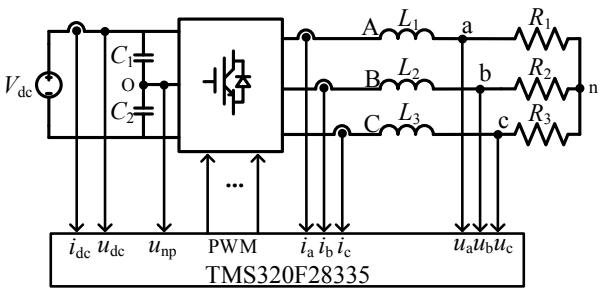
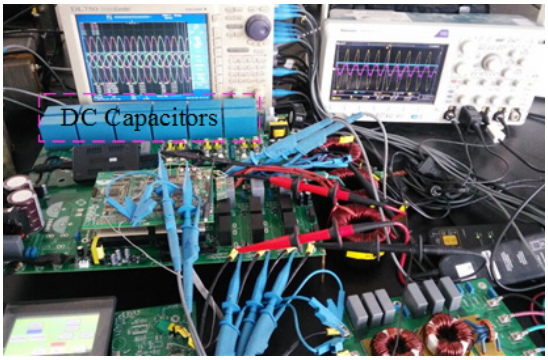


Fig. 11. The dynamic responses and FFT analysis under PF=1: (a) DC capacitor voltages; (b) Inverter output currents; (c) The FFT of the currents without the proposed strategy; (d) The FFT of the currents with the proposed strategy



(a)



(b)

Fig. 12. Experimental platform: (a) Schematic diagram of the experimental platform; (b) Experimental setup

Table 5. The parameters of experimental platform

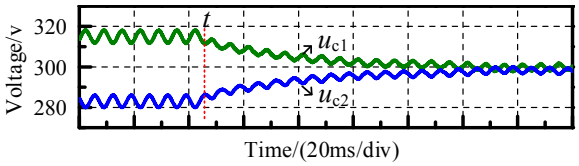
Parameters	Symbol	Value
DC voltage	V_{dc}	600V
Smoothing inductance	L_1,L_2,L_3	5.4mH
Load resistance	R_1,R_2,R_3	60Ω
Carrier frequency	f_s	16kHz
Modulation ratio	M	0.8
Fundamental frequency	f	50Hz

5.2 Experimental results

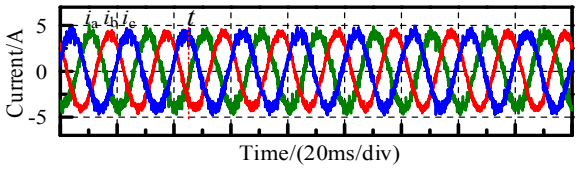
In order to verify the feasibility of the voltage difference feed-forward balancing control strategy, a TPTLTI experimental platform based on DSP is built as shown in Fig. 12 [18-20]. The platform parameters are shown in Table 5. Considering the imperfection of the DC capacitors and the attenuation effects of the capacitors during operation, the experiments are carried out with two cases: equal capacitances and unequal capacitances. The voltages and currents of the TPTLTI are recorded by a scope of DL750, and the FFT results are calculated by MATLAB.

5.2.1. Experimental results with equal capacitance

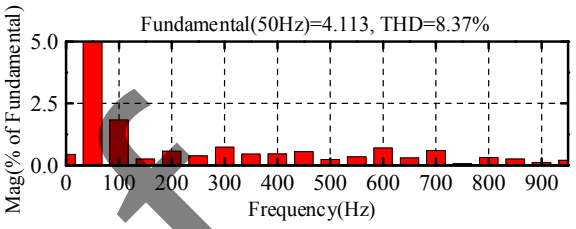
The experimental results with equal capacitances (C_1= C_2=300 μF) are shown in Fig. 13, the voltage difference feed-forward balance control strategy is triggered at time *t*. It can be seen from Fig. 13(a), the capacitor voltages are fluctuating with third-harmonics and the average voltage



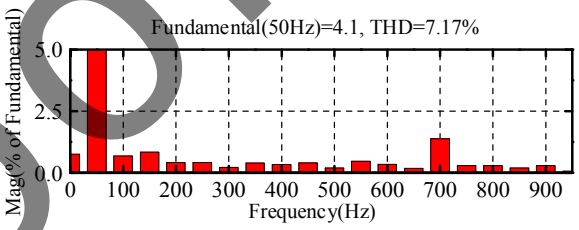
(a)



(b)



(c)



(d)

Fig. 13. Experimental results with equal capacitances. (a) DC capacitor voltages. (b) Inverter output currents. (c) The FFT of the currents without the proposed strategy. (d) The FFT of the currents with the proposed strategy

difference between two capacitors is 30 V when the neutral-point voltage balancing control is not applied. After triggering the strategy, the fluctuations of the capacitor voltages decrease, and the average voltage difference between two capacitors reduces to 0 V. Fig. 13(b) illustrates the inverter currents without and with the neutral-point voltage control. Fig. 13(c) and 13(d) are the FFT results of the inverter currents without and with the neutral-point voltage control. The THDs are 8.37% and 7.17%, respectively.

5.2.2. Experimental results with unequal capacitances

When C_1=350 μF and C_2=300 μF, the experimental results are shown in Fig. 14. The voltage difference feed-forward balance control strategy is triggered at time *t*. As shown in Fig. 14(a), the capacitor voltages are fluctuating with third-harmonics and the average voltage difference between two capacitors is 31V when the neutral-point

voltage balancing control is not applied. After triggering the strategy, the fluctuations of the capacitor voltages decrease, and the average voltage difference between two capacitors reduces to 0 V. Fig. 14(b) illustrates the inverter currents without and with the neutral-point voltage control. Fig. 14(c) and 14(d) are the FFT results of the inverter current without and with the neutral-point voltage balancing control. The THDs are 8.03% and 7.54%, respectively.

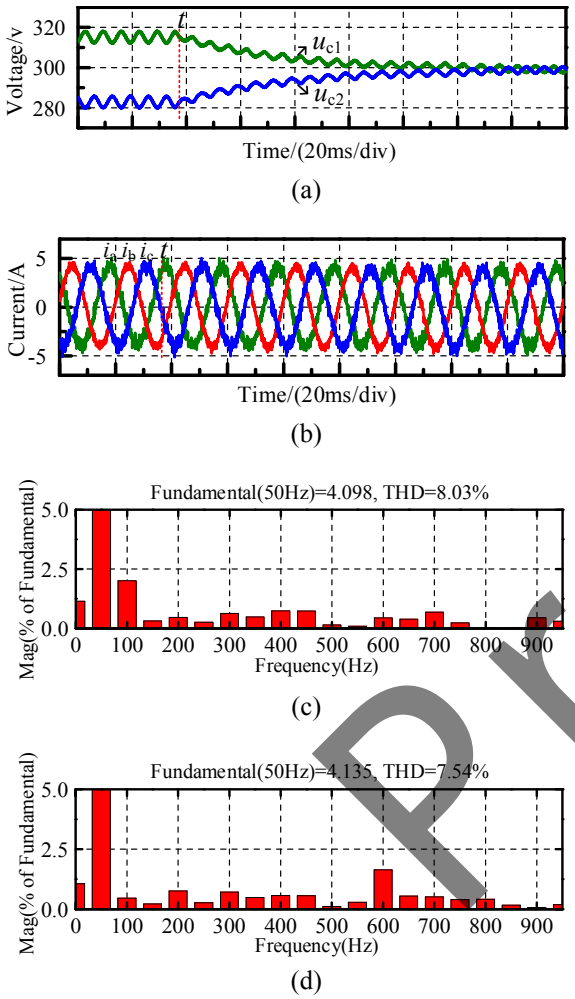


Fig. 14. Experimental results with unequal capacitances: (a) DC capacitor voltages; (b) Inverter output currents; (c) The FFT of the currents without the proposed strategy; (d) The FFT of the currents with the proposed strategy

The results from PSCAD simulations and experimental tests show that: 1) the fluctuations of the DC capacitor voltages are reduced; 2) the average voltages of the DC capacitors become equal; 3) the THDs of inverter currents are reduced; 4) the neutral-point voltage control of the TPTLTI is achieved.

The comparisons of the neutral-point voltage control strategies proposed in other literatures and this paper are summarized in Table 6 [21, 22].

6. Conclusions

In this paper, the mathematical model of a TPTLTI is derived, the fluctuating characteristics of capacitor voltages under different switching states and the mechanism of neutral-point voltage fluctuations are revealed. A feed-forward voltage balancing control strategy of DC-link capacitor voltages error is proposed. The proposed capacitor voltage balancing control strategy can be easily achieved through detecting the capacitor voltages. No need of measuring the neutral-point current and judging the operating states of the switches. The proposed capacitor voltage balancing control strategy can reduce the fluctuations of the capacitor voltages and the THDs of the output currents. The simulation and experimental results verify the correctness of the analysis of the problem of the neutral-point voltage fluctuations of TPTLTIs and the feasibility of the feed-forward capacitor voltage balancing control strategy.

However, the proposed strategy can only be applied with SPWM and the balancing capability of the proposed strategy is weak at high modulation indexes. The impacts of the proposed strategy on the power losses of TPTLTIs will be the future work.

Acknowledgements

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Table 6. Comparisons of the proposed strategy with other strategies

	Minimum Turn-on time Injection	Sixth-harmonic CMV Injection	New Modulation Strategy proposed in [9]	Proposed Strategy
Advantages	Strong balancing capability Applicable at pure reactive power	Proper balancing capability at any PFs	Strong balancing capability at any PFs and MIs	Strong balancing capability at high PFs and small MIs
Disadvantages	Weak balancing capability at low PFs and high MIs	The balancing capability dependents on output currents	Increase switching events	Weak balancing capability at high MIs
Output Distortions	Low impacts on THDs at any PFs	More impacts on THDs than “Minimum turn-on time Injection”	Increase THDs	Low impacts on THD at any PFs
Complexity	Moderate	Complexity	Moderate	Simple

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